REMARKS

The Office Action mailed on March 13, 2003, has been received and reviewed.

Claims 1 through 3, 5 through 41, and 43 through 55 are currently pending in the above-referenced application. Each of claims 1 through 3, 5 through 41, and 43 through 55 stands rejected.

Reconsideration of the above-referenced application is respectfully requested.

Rejections Under 35 U.S.C. § 103(a)

Each of claims 1 through 3, 5 through 41, and 43 through 55 stands rejected under 35 U.S.C. § 103(a).

It is respectfully submitted that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a), three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure.

Kim and Lin

Claims 1 through 3, 5 through 10, 15, 18, 19, 21, 22, 26 through 28, 30 through 36, 43, 44, and 50 through 52 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,004,867 to Kim et al. (hereinafter "Kim") in view of U.S. Patent 5,258,648 to Lin (hereinafter "Lin").

Kim teaches chip-scale packages and methods for forming such chip-scale packages. The chip-scale packages of Kim include a semiconductor device, or die, and a substrate. The substrate may comprise silicon. The substrate carries terminals and electrical. The terminals of the substrate are arranged correspondingly to the arrangement of bond pads on the semiconductor

device. *See, e.g.,* FIG. 2. The electrical traces reside within the substrate or therein. *See, e.g.,* FIG. 2; col. 3, lines 26-28; FIG. 3; col. 4, lines 47-51.

While Kim teaches that the conductive traces may be located anywhere *in* the substrate (col. 3, line 55) or at a surface of the substrate which is to be disposed against the semiconductor die (FIGs. 1 and 2), Kim does not teach or suggest that the conductive traces may be carried upon the other surface of the substrate, which other surface is to be located opposite a semiconductor device with which the substrate is to be assembled. To the contrary, the terminals and conductive traces are fabricated on an active surface of a semiconductor substrate, which ultimately becomes the bottom surface of the resulting substrate, by known semiconductor device fabrication processes. Col. 4, lines 13-18. Since conventional semiconductor device fabrication processes are used, material of the semiconductor substrate must be removed from the backside thereof, which ultimately becomes the top of the resulting substrate, so that terminals or other electrically conductive features may be exposed at both surfaces of the wafer. *See* FIG. 5D; col. 6, lines 19-21. Consequently, the only conductive features that are carried upon the surface of the substrate that is to be located opposite a semiconductor device are the terminals.

Lin teaches a composite flip chip semiconductor device. A flip chip semiconductor device refers to a package-less semiconductor device. Col. 1, lines 28-31. The device size is kept to a minimum since the device does not employ a traditional package body. Col. 1, lines 52-54. The conductive traces 26 of the interposer of Lin are carried on the surface of an interposer 22 which is to be coupled to the active surface of a semiconductor die. FIG. 1.

Independent claim 1 recites a chip-scale package which includes a semiconductor device and a substrate disposed adjacent an active surface of the semiconductor device. The substrate comprises a semiconductor material. At least one electrically conductive via extends at least partially through the substrate, is positioned over the semiconductor device, and communicates with a corresponding bond pad of the semiconductor device. In addition, at least one conductive trace, which is in communication with the at least one conductive via, is carried on a surface of the substrate which is *opposite* from the surface of the substrate that is adjacent to the semiconductor device.

Neither Kim nor Lin, either taken alone or in any combination thereof, teaches or suggests a conductive trace carried on the surface of a substrate in a chip scale package which is to be positioned opposite from (*i.e.,* facing away from) the semiconductor device to establish a *prima facie* case of obviousness regarding the claimed invention under 35 U.S.C. § 103(a). Rather, Kim teaches conductive traces carried within the substrate or on a surface thereof which is to be disposed against a semiconductor device, and Lin teaches conductive traces carried on the surface of an interposer between the substrate and a package-less semiconductor device.

Accordingly, it is respectfully submitted that, under 35 U.S.C. § 103(a), independent claim 1 is allowable over the combination of Kim and Lin because any combination of such prior art, at the very least, does not teach or suggest all the claim limitations to establish a *prima facie* case of obviousness regarding the claimed invention under 35 U.S.C. § 103(a).

Claims 2, 3, 5 through 10, 15, 18, and 19 are each allowable, among other reasons, as depending from independent claim 1, which is allowable.

Independent claim 21 recites a chip-scale package with a substrate having a first surface with contact areas corresponding to an arrangement of bond pads on a semiconductor device to be assembled therewith and a second surface with at least one conductive trace thereon. Neither Kim nor Lin, alone or in any combination teaches or suggests a package with a substrate which includes conductive traces on a surface thereof that is to be located opposite from a semiconductor device to establish a *prima facie* case of obviousness regarding the claimed invention under 35 U.S.C. § 103.

Therefore, it is respectfully submitted that, under 35 U.S.C. § 103(a), independent claim 21 is allowable over the combination of Kim and Lin because the combination of the cited prior art, at the very least, does not teach or suggest the claim limitations of the claimed invention to establish a *prima facie* case of obviousness regarding the claimed invention under 35 U.S.C. § 103(a).

Claims 22, 26 through 28, and 30 through 36 are each allowable, among other reasons, as depending from independent claim 21, which is allowable.

Neither Kim nor Lin, taken alone or in any combination thereof, teaches or suggests a carrier with at least one via that extends from a first surface of the carrier, adjacent to which a

semiconductor device is to be positioned, to a second surface of the carrier, by which at least one conductive trace that extends laterally from an end of the via is carried, as recited in independent claim 43 to establish a *prima facie* case of obviousness regarding the claimed invention under 35 U.S.C. § 103(a). Rather, the teachings of Kim and Lin are limited to substrates and interposers that include conductive traces on surface thereof that are to be positioned adjacent to a semiconductor device.

Therefore, it is respectfully submitted that, under 35 U.S.C. § 103(a), independent claim 43 is allowable over the combination of Kim and Lin because the combination of the cited prior art does not teach or suggest all the claim limitations of the claimed invention to establish a *prima facie* case of obviousness regarding the claimed invention under 35 U.S.C. § 103(a).

Claims 44 and 50 through 52 are each allowable, among other reasons, as depending from independent claim 43, which is allowable.

Kim, Lin, and Gnadinger

Claims 11 through 14, 20, 23 through 25, 37 through 41 and 45 through 49 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kim and Lin and, further. in view of U.S. Patent 5,229,647 to Gnadinger.

Claims 11 through 14 and 20 are each allowable, among other reasons, as depending either directly or indirectly from independent claim 1, which is allowable.

Claims 23 through 25 and 37 through 41 are each allowable, among other reasons, as depending either directly or indirectly from independent claim 21, which is allowable.

Each of claims 45 through 49 is allowable, among other reasons, as depending either directly or indirectly from independent claim 43, which is allowable.

Further, Gnadinger, which teaches wafers with vias that extend completely therethrough, but which lacks any teaching or suggestion of conductive traces on the surfaces thereof that are to be located opposite a semiconductor device to be assembled therewith, does not remedy any of the aforementioned deficiencies of Kim and Lin to establish a *prima facie* case of obviousness regarding the claimed invention under 35 U.S.C. § 103.

Kim and Lin

Claims 16, 17, 29, and 53 through 55 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kim and Lin.

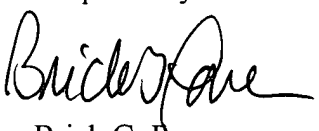
Claims 16, 17, 29 and 53 through 55 are each allowable, among other reasons, as depending from one of independent claims 1, 21, or 43, each of which is allowable.

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 1-3, 5 through 41, and 43 through 55 be withdrawn.

CONCLUSION

It is respectfully submitted that each of claims 1 through 3, 5 through 41, and 43 through 55 is allowable. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,



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